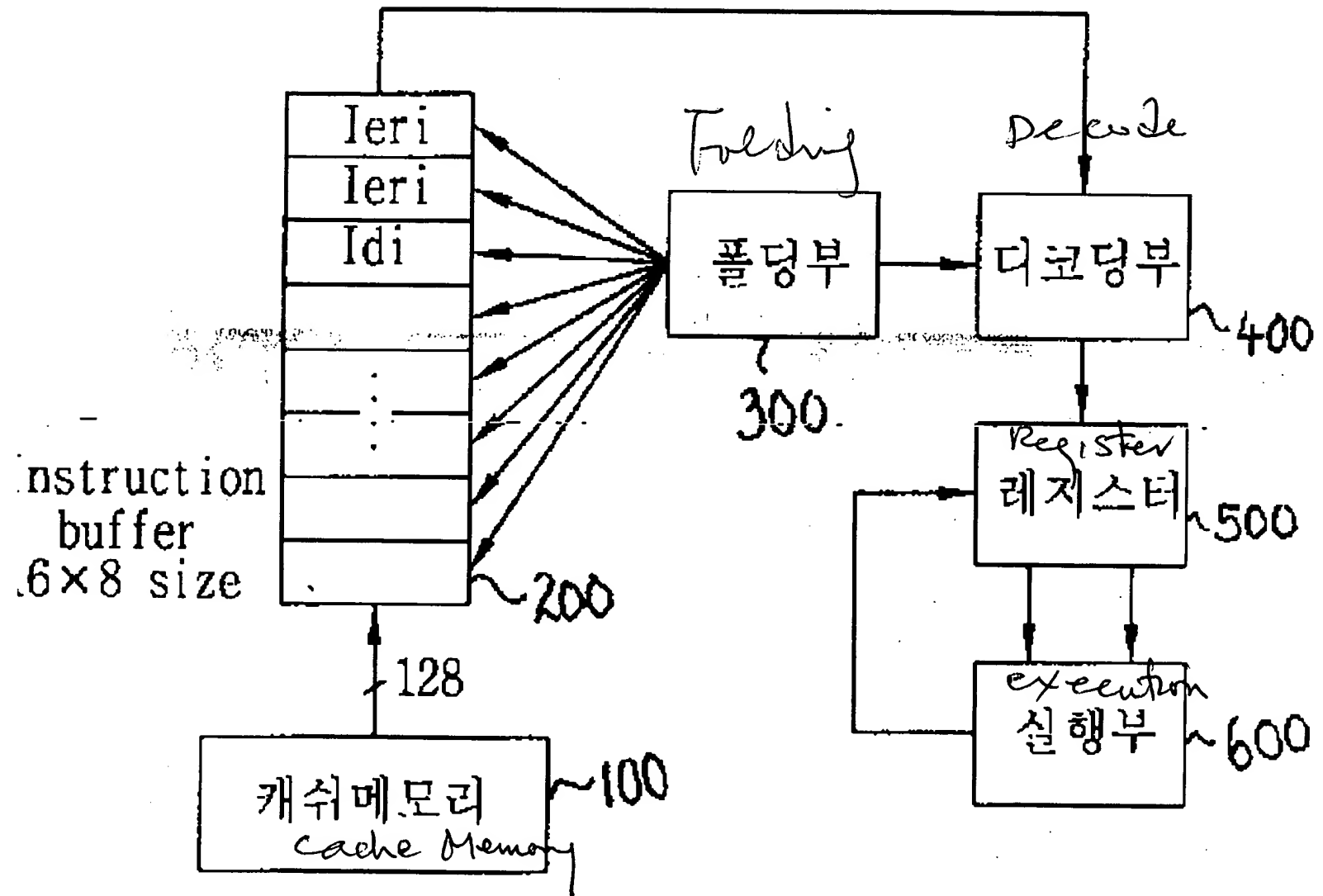


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# United States Patent [19]

Jeremiah

[11] Patent Number: 5,398,321  
[45] Date of Patent: Mar. 14, 1995

## [54] MICROCODE GENERATION FOR A SCALABLE COMPOUND INSTRUCTION SET MACHINE

[75] Inventor: Thomas L. Jeremiah, Endwell, N.Y.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 184,401

[22] Filed: Jan. 21, 1994

### Related U.S. Application Data

[63] Continuation of Ser. No. 653,006, Feb. 8, 1991, abandoned.

[51] Int. Cl.<sup>6</sup> ..... G06F 9/22; G06F 9/38

[52] U.S. Cl. .... 395/375; 364/DIG. 1; 364/DIG. 2; 364/231.8; 364/230; 364/931.41; 364/946.9; 364/948.3; 364/262.4

[58] Field of Search ..... 395/375

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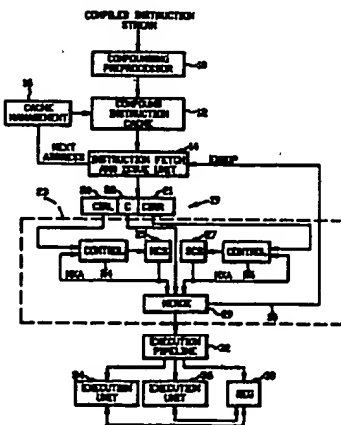
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### [57] ABSTRACT

An apparatus for generating microcode in a scalable compound instruction set machine operates in response to compounding information indicating that two or more adjacent instructions are to be executed in parallel. Separate and independent microcode is held in control store for each possible instruction in a group. Microcode sequences for each instruction of a group of instructions to be executed in parallel are merged in response to the compounding information into a single microinstruction sequence.

9 Claims, 7 Drawing Sheets





## Eickemeyer et al.

**[11] Patent Number: 5,197,135**

**[45] Date of Patent: Mar. 23, 1993**

- [54] MEMORY MANAGEMENT FOR SCALABLE  
COMPOUND INSTRUCTION SET  
MACHINES WITH IN-MEMORY  
COMPOUNDING**

- [75] **Inventors:** Richard J. Elckemeyer, Endicott; Stamatis Vassiliadis, Vestal; Bartholomew Blaner, Newark Valley, all of N.Y.

- [73] Assignee: International Business Machines Corporation, Armonk, N.Y.**

- [21] Appl. No.: 543,458**

- [22] Filed: Jun. 26, 1990**

- [51] Int. Cl.<sup>5</sup> ..... G06F 9/38

- [52] U.S. Cl. .... 395/375; 395/800;  
364/DIG. 1; 364/262.4; 364/262.9; 364/263;  
364/261; 364/261.1; 364/261.2

- [58] **Field of Search** ..... 395/375, 800, 775, 650

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**Attorney, Agent, or Firm—Baker, Maxham, Jester & Meador**

## [57] ABSTRACT

A digital computer system is described which is capable of processing 2 or more computer instructions in parallel and which has the capability of generating compounding tag information for those instructions, the compounding tag information being associated with instructions for the purpose of indicating groups of instructions which are to be concurrently executed. A compounding tag has a value which indicates the size of the group of instructions which are to be concurrently executed. The computer system includes a hierarchially-arranged memory which provides instructions to a CPU for execution. The instructions are compounded in the memory, and provision is made in the memory for storage of their compounding tags. In the event of modification of an instruction in memory, the invention provides for reduction of the value of the compounding tags for the modified instruction and instructions which are capable of being compounded with the modified instruction or for generation of new tag values for the modified instruction and instructions which are adjacent it in memory.

**15 Claims, 15 Drawing Sheets**

